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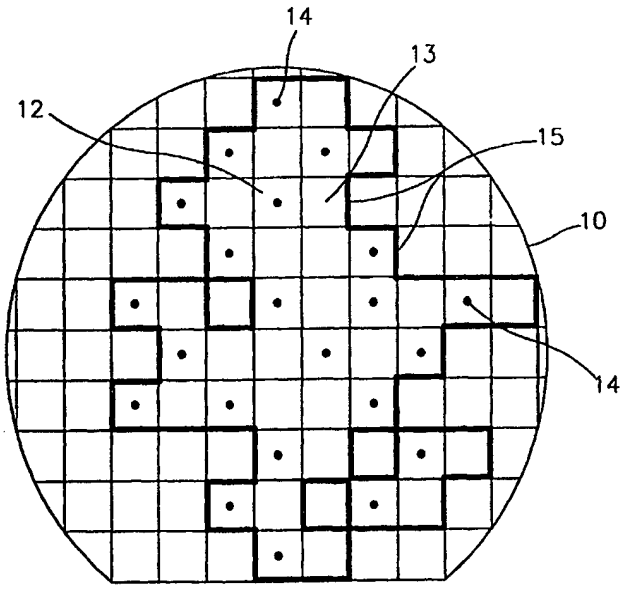
(54) Title: METHOD FOR MEASURING NUMBER OF YIELD LOSS CHIPS AND NUMBER OF POOR CHIPS BY TYPE DUE TO DEFECT OF SEMICONDUCTOR CHIPS

(57) Abstract

A method for measuring the number of yield loss chips and the number of poor chips by type due to defects of semiconductor chips by which it is possible to remarkably improve the yield of semiconductor chips by measuring the number of yield loss chips due to defects of the chips, the maximum number of yield loss chips, and the number of the specific type of poor chips in an arbitrary process, an arbitrary equipment, and an arbitrary process section among semiconductor fabrication processes, thus managing the defects of the chips, is provided. The method for measuring the number of yield loss chips and the number of poor chips by type due to defects of semiconductor chips includes the steps of checking defective chips among effective chips on a wafer which underwent a predetermined process using a defect examination equipment and plotting the checked defective chips on a first wafer map, forming disparity chips by pairing defective chips and non–defective chips adjacent to the defective chips on the first wafer map and determining a maximum reliability region formed of regions in which the disparity chips are located, plotting good chips and poor chips by type on a second wafer map using a yield measuring apparatus after completing the process, and classifying the number of good chips and poor chips by type on the second wafer map corresponding to the defective chips and the non–defective chips in the maximum reliability region on the first wafer map.



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METHOD FOR MEASURING NUMBER OF YIELD LOSS CHIPS AND NUMBER OF POOR CHIPS BY TYPE DUE TO DEFECT OF SEMICONDUCTOR CHIPS

Technical Field

The present invention relates to a method for measuring an accurate value of yield loss due to chip defect caused by the inflow of dust or foreign material or due to poor shapes of chips during semiconductor manufacturing processes.

Background Art

Defects of wafer chips caused by dust, foreign material, and poor shapes of the chips during semiconductor manufacturing processes critically affect the yield and characteristics of chips. Such a defect is generated in all handling processes including environment as well as all equipments and all semiconductor manufacturing processes. Thus, this makes the range of management of defects required by field managers very broad. Accordingly, production and quality management of chips is difficult.

Defects of chips critically affect the yield loss and characteristics of the chips. The yield loss is generally 1 through 30% of defective chips. Namely, the degree of yield loss varies according to processes with respect to the same numbers of defective chips. The degree of the yield loss varies according to products. The degree of the yield loss varies according to the degree and type of defects.

For example, in the case of a dynamic random access memory (DRAM), a poor chip is obtained when a defect exists outside a memory cell region. However, when a defect exists inside the memory cell region, a good chip can be obtained by performing a laser repair using a redundancy cell. Namely, the degree of yield loss varies in the same chip according to the positions of the defect.

Since the causes of yield loss during the fabrication of the

semiconductor chips are derived from all processes such as a photolithography process, an etching process, a diffusion process, an ion implantation process, and a thin film deposition process as well as the above defects, it is difficult to determine how much effect defects have on yield loss.

It is difficult to manage yield by managing defects since the degree of yield loss varies according to products when defects are generated, the degree of the yield loss varies according to processes with respect to the same product, and defects are generated in all processes, equipments, circumstances, and handling processes of a semiconductor fabrication field.

It is possible to measure the total number of defects generated on a wafer, the total number of defective chips by the degree and type of defects with current technology of measuring yield loss and characteristics of the chip according to the defects. It is possible to analyze and measure the amount of yield loss to the total number of defects, the number of specific poor chips to the total number of defects, the yield loss amount to the total number of defective chips, and the number of specific poor chips to the total number of defective chips by matching the measurement result to the yield measurement result and statistically processing the result.

Accordingly, when the total number of defects or the total number of defective chips increases, the yield loss amount and specific defect ratio also increase. Namely, it is possible to relatively measure the amount of yield loss to the total number of defects, the number of specific poor chips to the total number of defects, the yield loss amount to the total number of defective chips, and the number of specific poor chips to the total number of defective chips.

As mentioned above, since the causes of yield loss exist in all processes, it is not possible to measure the absolute value of the yield loss by which it is possible to determine how much the chips in which the yield loss occurs are affected by the defect.

Disclosure of the Invention

It is a first object of the present invention to provide a method for measuring the number of yield loss chips and the number of poor chips by type due to the defects of semiconductor chips by which it is possible to remarkably improve the yield of semiconductor chips by accurately obtaining the number of the yield loss chips due to defects of the chips, the maximum number of yield loss chips, and the number of specific types of poor chips in an arbitrary process, an arbitrary equipment, and an arbitrary process section among semiconductor fabrication processes, thus managing the defects of the chips.

It is a second object of the present invention to provide a computer readable medium on which the above method realized as a program is recorded.

Accordingly, to achieve the first object, there is provided a method for measuring the number of yield loss chips and the number of poor chips by type due to defects of semiconductor chips, comprising the steps of checking defective chips among effective chips on a wafer which underwent a predetermined process using a defect examination equipment and plotting the checked defective chips on a first wafer map, forming disparity chips by pairing defective chips and non-defective chips adjacent to the defective chips on the first wafer map and determining a maximum reliability region formed of regions in which the disparity chips are located, plotting good chips and poor chips by type on a second wafer map using a yield measuring apparatus after completing the process, and classifying the number of good chips and poor chips by type on the second wafer map corresponding to the defective chips and the non-defective chips in the maximum reliability region on the first wafer map.

Accordingly, to achieve the second object, there is provided a computer readable medium including program commands for measuring the number of the yield loss chips and the number of poor chips by type due to the defect of semiconductor chips, the computer readable medium

comprising a computer readable code for inputting data on defective chips and non-defective chips among effective chips on a wafer which underwent a predetermined process from a defect examination equipment and plotting the input data on the defective chips and the non-defective chips on a first wafer map, a computer readable code for forming disparity chips by pairing the defective chips and the non-defective chips adjacent to the defective chips on the first wafer map and determining the maximum reliability region comprised of regions in which the disparity chips are located, a computer readable code for inputting data on good chips and poor chips by type from a yield measuring apparatus and plotting the input data on the good chips and the poor chips on a second wafer map, and a computer readable code for classifying the number of the good chips and the poor chips by type on the second wafer map corresponding to the defective chips and the non-defective chips in the maximum reliability region on the first wafer map and mapping out the statistics with respect to the yield loss and the number of the poor chips by type.

Brief Description of the Drawings

The above objects and advantages of the present invention will become more apparent by describing in detail a preferred embodiment thereof with reference to the attached drawings in which:

FIG. 1 shows a wafer map on which defective chips among effective chips are plotted on a wafer using a defect examination equipment according to the present invention;

FIG. 2 shows a wafer map on which disparity chips are formed based on a defective chip pattern according to the present invention;

FIG. 3 explains a method of constituting the disparity chips according to the present invention;

FIG. 4 shows a wafer map on which a maximum reliability region fixed by the combination of disparity chips according to the present invention is displayed;

FIG. 5 shows a wafer map on which effective chips on a wafer are classified into good chips and poor chips using a yield measuring apparatus according to the present invention; and

FIG. 6 shows a wafer map on which good chips and poor chips by type in the maximum reliability region according to the present invention are extracted.

Best mode for carrying out the Invention

Hereinafter, an embodiment of the present invention will be described in detail with reference to the attached drawings.

In an embodiment of the present invention, in the first step, defective chips among effective chips on a wafer are plotted on a first wafer map using a defect examination equipment as shown in FIG. 1. FIG. 1 shows a first wafer map on which an effective chip region 11 comprised of 77 chips is constituted of twenty-two (22) defective chips 12 having defects 14 and fifty-five (55) non-defective chips 13 on a wafer 10.

In the second step referred to by FIG. 2, a disparity chip 15 is formed on the first wafer map by pairing each defective chip 12 confirmed in the first step and each non-defective chip 13 adjacent thereto.

In FIG. 3, a disparity chip is formed by sequentially searching for defective chips on the wafer map and combining the defective chips with non-defective chips directly above, below, to the left and right among the non-defective chips which did not form the disparity chip 15. Since the defective chips are collectively generated, the defective chips which do not form the disparity chip 15, that is, a non-disparity chip 16 can deteriorate reliability. Therefore, the non-disparity chip 16 is excluded from data which form the reliability region for generating statistics according to the present invention.

In the third step, referring to FIG. 4, a maximum reliability region 17 formed by combining the disparity chips formed in the second step is fixed on the first wafer map.

In the fourth step, referring to FIG. 5, good chips A and poor chips B, C, D, E, and F are plotted on the second wafer map using the yield measuring apparatus. FIG. 5 shows the second wafer map on which good chips and poor chips are plotted.

In the fifth step, referring to FIG. 6, good chips A and poor chips B, C, D, E, and F on the second wafer map, resulting from the measurement of the yield in the fourth step are extracted from the maximum reliability region on the first wafer map.

In the sixth step, as shown in Table 1, all the disparity chips in the maximum reliability region are classified into defective chips and non-defective chips. The classified defective chips and non-defective chips are respectively classified into good chips, poor chips, and inferiority types.

[TABLE 1]

	Number of good chips	Number of poor chips	Total	Inferiority types				
				B	C	D	E	F
Defective chips	12	10	22	4	3	1	1	1
Non-defective chips	15	7	22	2	2	1	1	1

In the seventh step, the generation ratios of the good chips and the poor chips to the defective chips and the generation ratios according to inferiority types and generation ratio of good chips and poor chips to non-defective chips and the generation ratios according to inferiority types are calculated as follows.

Defective chips:

The generation ratio of good chips : 12/22 = 0.545 (a)

The generation ratio of poor chips : 10/22 = 0.455 (b)

The generation ratio of B type inferiority : 4/22 = 0.182 (c)

The generation ratio of C type inferiority : 3/22 = 0.136 (d)

The generation ratio of D type inferiority : 1/22 = 0.045 (e)

The generation ratio of E type inferiority : 1/22 = 0.045 (f)

The generation ratio of F type inferiority : 1/22 = 0.045 (g) Non-defective chips:

The generation ratio of good chips : 15/22 = 0.682 (h)

The generation ratio of poor chips : 7/22 = 0.318 (i)

The generation ratio of B type inferiority : 2/22 = 0.091 (j)

The generation ratio of C type inferiority : 2/22 = 0.091 (k)

The generation ratio of D type inferiority : 1/22 = 0.045 (l)

The generation ratio of E type inferiority : 1/22 = 0.045 (m)

The generation ratio of F type inferiority : 1/22 = 0.045 (n)

In step 8, the sum of yield losses according to the current level, the optimal level, and the worst level is calculated by the process provided in Table 2 using the various generation ratios calculated in the step 7.

[TABLE 2]

	Total number of chips	Number of non-defective chips	Yield loss of non-defective chips	Sum of yield losses
		Number of defective chips	Yield loss of defective chips	
Current level	77	55	17.49 (55×0.318)	27.5 (o)
		22	10.01 (22×0.455)	
Optimal level	77	77	24.49 (77×0.318)	24.49 (p)
		0	0 (0×0.455)	
Worst level	77	0	0 (0×0.318)	35.04 (q)

		77	35.04 (77×0.455)	

Current level refers to a state in which there are fifty-five (55) non-defective chips and twenty-two (22) defective chips. Optimal level refers to a state in which all chips are non-defective chips. Worst level refers to a state in which all chips are defective chips.

In the ninth step, the number of yield loss chips according to defects and the maximum number of yield loss chips are calculated as follows based on the sum of yield losses obtained in step 8.

The number of yield loss chips due to defects = the current level value (o) - the optimal level value (p) = 27.5 - 24.49 = 3.01 chips

The maximum number of yield loss chips = the worst level value (q) - the optimal level value (p) = 35.04 - 24.49 = 10.55 chips

Here, in the current level (the total number of chips : 77 and the number of the defective chips : 22), the yield loss (3.01/77 = 3.91%) of the 3.01 chips is generated due to the defects. A maximum yield loss (10.55/77 = 13.7%) of 10.55 chips may be generated by the defects.

It is possible to produce processes of inferiority generation of the current level, the optimal level, and the worst level according to the inferiority type from the various generation ratios calculated in the seventh step. The total number of B-type poor chips according to the current level, the optimal level, and the worst level in the inferiority type B are calculated by the processes provided in Table 3.

[TABLE 3]

	Total number of chips	Number of non-defective chips	Number of B type poor chips of non-defective chips	Total number of B type poor chips

		Number of defective chips	Number of B type poor chips of defective chips	
Current level	77	55	5.01 (55×0.091)	9.01 (o)
		22	4.00 (22×0.182)	
Optimal level	77	77	7.01 (77×0.091)	7.01 (p)
		0	0 (0×0.182)	
Worst level	77	0	0 (0×0.091)	14.01 (q)
		77	14.01 (77×0.182)	

It is possible to obtain the generation ratio of B-type inferiority and the maximum generation ratio of B-type inferiority.

The number of chips in which B-type specific inferiority is generated due to defects = the current level value (r) - the optimal level value (s) = 9.01 - 7.01 = 2 chips

The maximum number of chips in which the B type specific inferiority may be generated = the worst level value (t) - the optimal level value (s) = 14.01 - 7.01 = 7 chips

It is noted from the above that the B-type of inferiority (2/77 = 2.60%) is generated in two chips due to the defects in the current level (the total number of chips: 77 and the number of the defective chips: 22) and that the B-type of inferiority (7/77 = 9.09%) may be generated in a maximum of 7 chips due to the defects.

Also, the total number of C-type poor chips according to the current level, the optimal level, and the worst level in the C type inferiority type can

be calculated by the processes provided in Table 4.

[TABLE 4]

	Total number of chips	Number of non-defective chips	Number of C type poor chips of non-defective chips	Total number of C type poor chips
		Number of defective chips	Number of C type poor chips of defective chips	
Current level	77	55	5.01 (55×0.091)	8.00 (u)
		22	2.99 (22×0.136)	
Optimal level	77	77	7.01 (77×0.091)	7.01 (v)
		0	0 (0×0.136)	
Worst level	77	0	0 (0×0.091)	10.47 (w)
		77	10.47 (77×0.136)	

It is possible to obtain the generation ratio of C-type inferiority and the maximum generation ratio of C-type inferiority.

The number of chips in which C-type inferiority is generated due to defects = the current level value (u) - the optimal level value (v) = 8.00 - 7.01 = 0.99 chips

The maximum number of chips in which C-type inferiority may be generated = the worst level value (w) - the optimal level value (v) = 10.47 -

7.01 = 3.46 chips

It is noted from the above that the C-type of inferiority (0.99/77 = 1.29%) is generated in 0.99 chips due to the defects in the current level (the total number of chips: 77 and the number of the defective chips: 22) and that the C-type of inferiority (3.46/77 = 4.49%) may be generated in a maximum of 3.46 chips due to the defects.

Also, it is possible to obtain the inferiority generation ratio and the maximum inferiority generation ratio by the same method as used in the B-type and C-type of inferiority.

The above-mentioned embodiment can be made out as a program which can be executed by computers. The embodiment can be realized by general purpose digital computers which operate program from a computer readable medium. The computer readable medium may include a magnetic storing medium such as a ROM, a floppy disk, and a hard disk, an optical reading medium such as a CD-ROM and a DVD, and carrier waves, for example, transmission through the Internet.

Functional programs, codes, and code segments for realizing the present invention can be easily referred to by programmers in the art.

Industrial Applicability

As mentioned above, according to the present invention, it is possible to accurately measure the absolute values of the yield loss and the specific inferiority types due to the defects by clarifying the yield loss process after completely removing the influences of other process elements than the defects through a maximum reliability region design method constituted of only the disparity chip. Therefore, it is possible to accurately check the yield loss due to defects with respect to a unit process, a unit equipment, and a unit process section on the basis of the absolute values. Accordingly, it is possible to set the management order of priority and the management level with respect to critical processes, critical equipment, and critical process sections by correct numbers, to thus reasonably manage

defects. Accordingly, it is possible to improve yield.

What is claimed is:

1. A method for measuring the number of yield loss chips and the number of poor chips by type due to defects of semiconductor chips, comprising the steps of:

(a) checking defective chips among effective chips on a wafer which underwent a predetermined process using a defect examination equipment and plotting the checked defective chips on a first wafer map;

(b) forming disparity chips by pairing defective chips and non-defective chips adjacent to the defective chips on the first wafer map and determining a maximum reliability region formed of regions in which the disparity chips are located;

(c) plotting good chips and poor chips by type on a second wafer map using a yield measuring apparatus after completing the process; and

(d) classifying the number of good chips and poor chips by type on the second wafer map corresponding to the defective chips and the non-defective chips in the maximum reliability region on the first wafer map.

2. The method of claim 1, wherein, in the step (b), disparity chips are formed by sequentially searching defective chips on a wafer map and by combining the defective chip searched among non-defective chips which did not form a disparity chip with non-defective chips directly above, below, to the left and right and the defective chips which are not combined with the adjacent non-defective chips among the searched defective chips are excluded from the maximum reliability region.

3. The method of claim 1, wherein the step (d) comprises the steps of:

(d1) classifying the number of good chips and poor chips on a second wafer map, corresponding to defective chips and non-defective chips in the maximum reliability region on a first wafer map; and

(d2) obtaining the generation ratio of poor chips and inferiority

generation ratio by type to the defective chips and the generation ratio of the poor chips and the inferiority generation ratio by type to the non-defective chips based on the number of good chips and poor chips by type classified in the step (d1).

4. The method of claim 3, wherein the step (d) further comprises the step of (d3) obtaining the sum of the yield loss according to a current level, an optimal level, and a worst level and the total number of poor chips by type, based on the generation ratio of poor chips and inferiority generation ratio by type to the defective chips and the generation ratio of the poor chips and the inferiority generation ratio by type to the non-defective chips.

5. The method of claim 4, wherein the step (d) further comprises the step of (d4) obtaining the number of yield loss chips, the maximum number of yield loss chips, and the ratio of the maximum number of yield loss chips to the number of yield loss chips and the number of chips in which inferiority is generated by type, the maximum number of chips in which inferiority may be generated, and the ratio of the maximum number of chips in which inferiority may be generated to the number of chips in which inferiority is generated by type.

6. A computer readable medium including program commands for measuring the number of the yield loss chips and the number of poor chips by type due to the defect of semiconductor chips, the computer readable medium comprising:

(a) a computer readable code for inputting data on defective chips and non-defective chips among effective chips on a wafer which underwent a predetermined process from a defect examination equipment and plotting the input data on the defective chips and the non-defective chips on a first wafer map;

(b) a computer readable code for forming disparity chips by pairing the defective chips and the non-defective chips adjacent to the defective chips on the first wafer map and determining the maximum reliability region comprised of regions in which the disparity chips are located;

(c) a computer readable code for inputting data on good chips and poor chips by type from a yield measuring apparatus and plotting the input data on the good chips and the poor chips on a second wafer map; and

(d) a computer readable code for classifying the number of the good chips and the poor chips by type on the second wafer map corresponding to the defective chips and the non-defective chips in the maximum reliability region on the first wafer map and mapping out the statistics with respect to the yield loss and the number of the poor chips by type.

FIG. 1

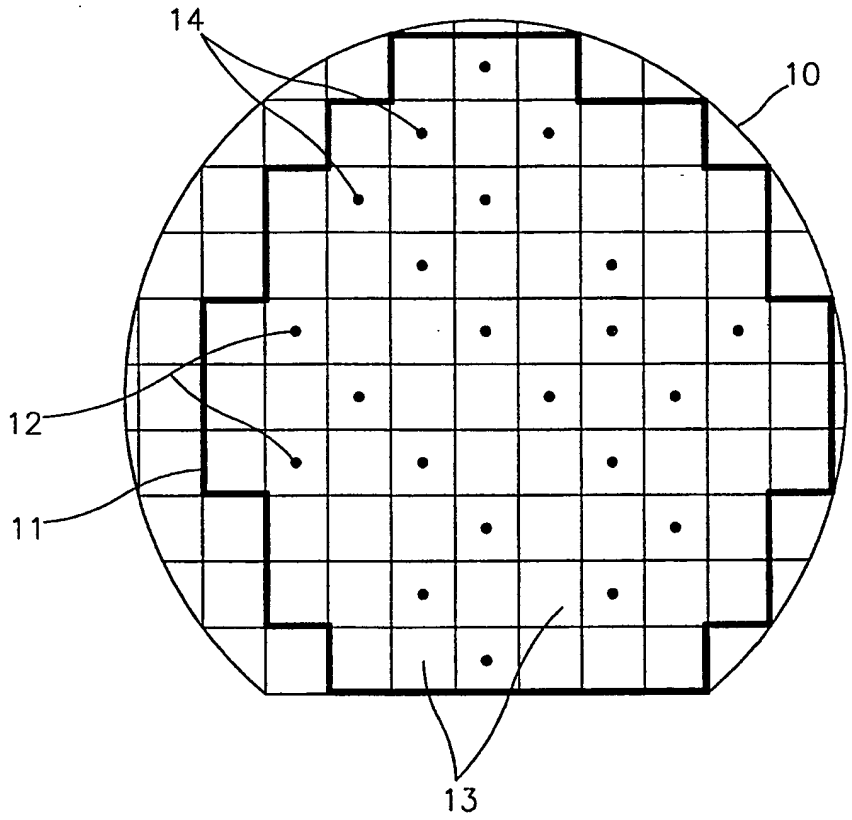


FIG. 2

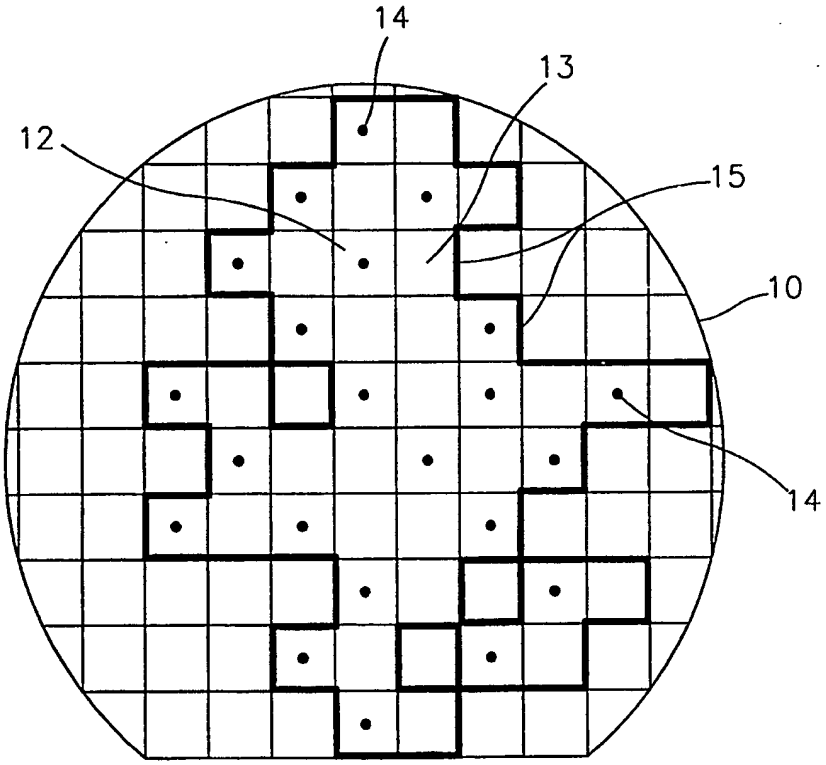


FIG. 3

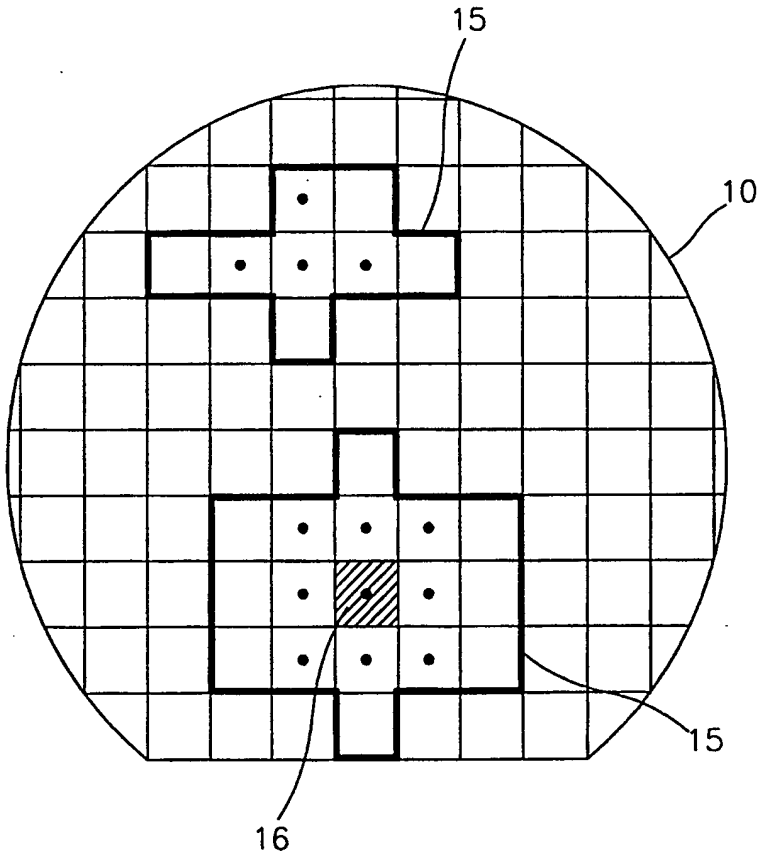


FIG. 4

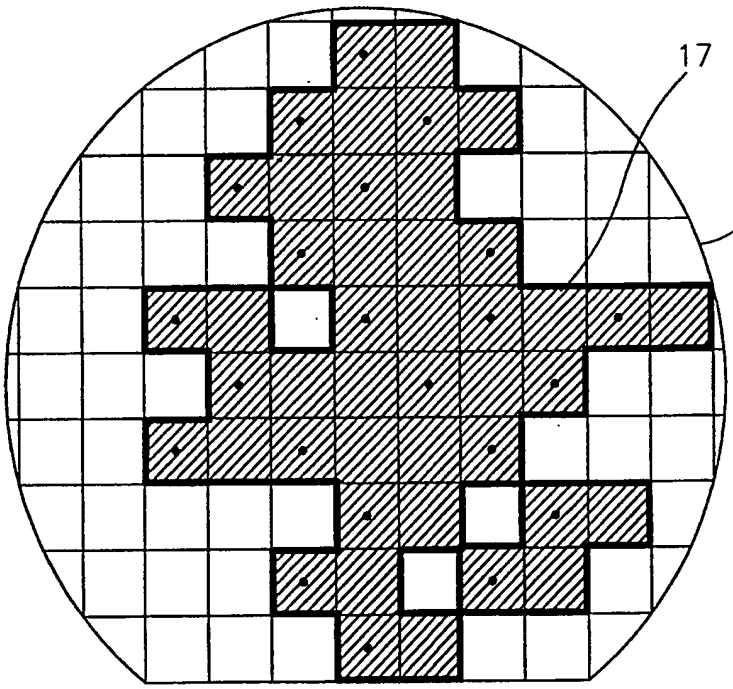
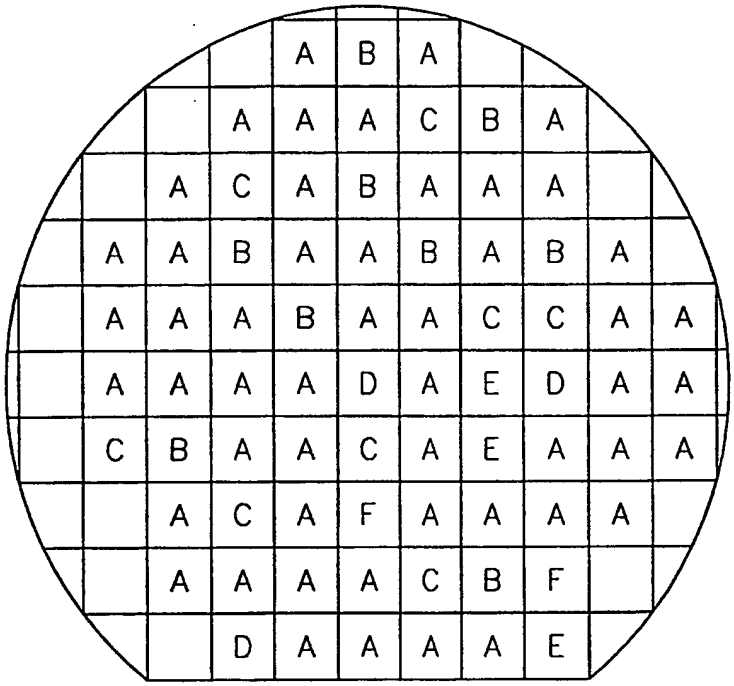
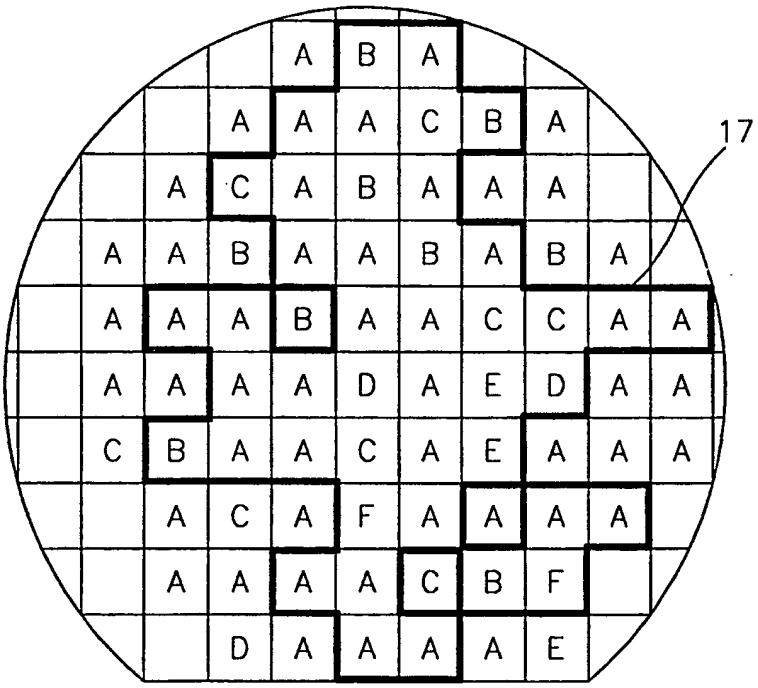


FIG. 5



A : GOOD CHIPS
B,C,D,E,F : POOR CHIPS BY TYPE

FIG. 6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A C A F A A A A
A A A A C B F
D A A A A E

INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR 99/00383

A. CLASSIFICATION OF SUBJECT MATTER

IPC[7]: H 01 L 21/66

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5665609 A (MORI) 09 September 1997 (09.09.97) abstract, claims 1-3.	1-6
A	JP 06-310581 A (HITACHI LTD.) 04 November 1994 (04.11.94) (abstract).[online] [retrieved on 09 November 1999 (09.11.99)]. Retrieved from: PAJ-Database, abstract.	1-5
A	Hansen C., Theyrgod P., "Use of wafer maps in integrated circuit manufacturing." [online], In:Microelectronics Reliability, vol.38, no.6-8, pp. 1155-1164, June 1998 [retrieved on 09 November 1999 (09.11.99)], Retrieved from: Inspec-Database, abstract.	1-6
AP	US 5787190 A (PENG et al.) 28 July 1998 (28.07.98) abstract, claims 1-3.	1-5

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Date of the actual completion of the international search	Date of mailing of the international search report
10 November 1999 (10.11.99)	03 December 1999 (03.12.99)
Name and mailing adress of the ISA/AT Austrian Patent Office Kohlmarkt 8-10; A-1014 Vienna Facsimile No. 1/53424/200	Authorized officer Mayer Telephone No. 1/53424/452

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR 99/00383

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